

Figure 1A

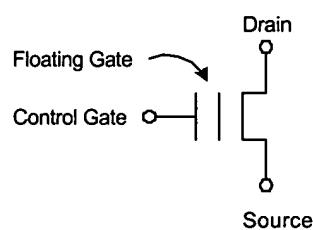


Figure 1B

0.0 0.2 0.4 0.6 0.8 1.0 1.2 1.4 1.6 1.8 2.0 2.2 2.4 2.6 2.8 3.0 3.2 3.4 3.6 3.8 4.0

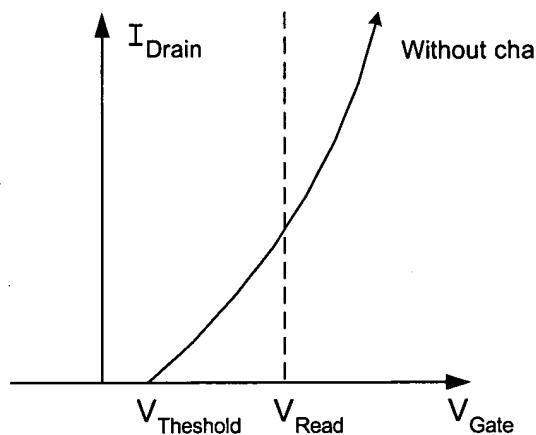


Figure 1C

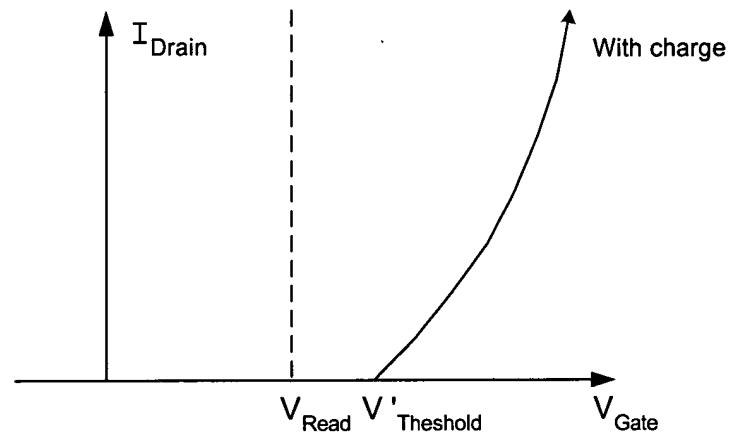
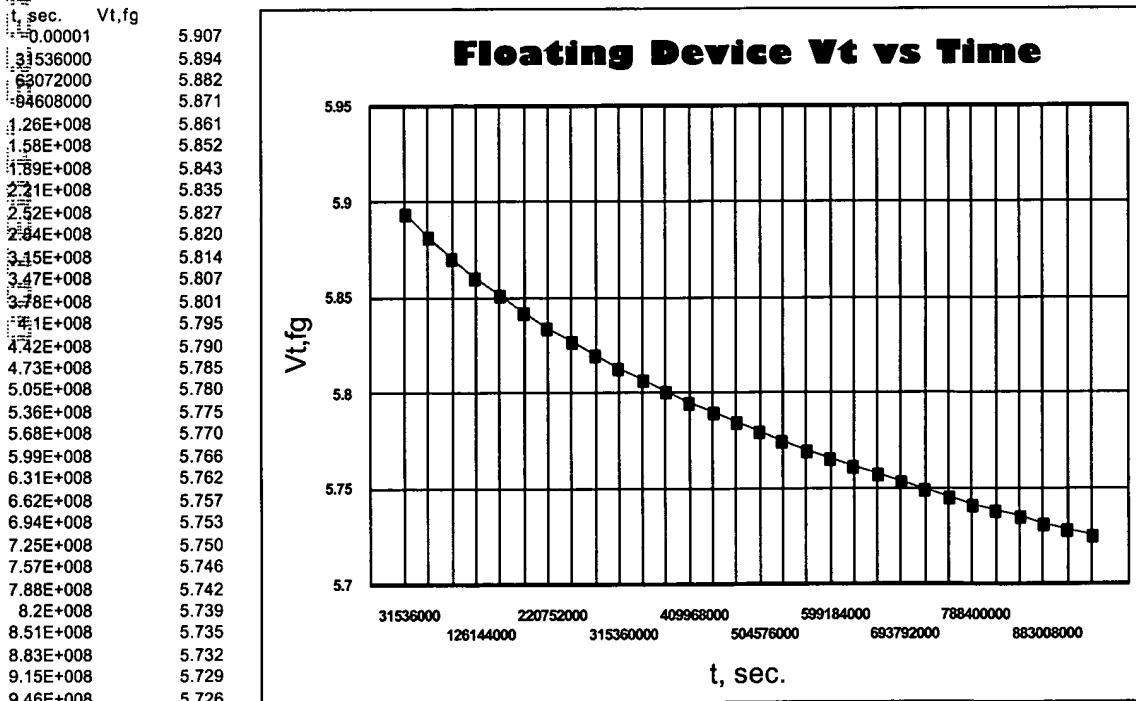


Figure 1D

Calculation of memory cell retention characteristics

						Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s		31536000	1 year
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.054588E-034		94608000	3 years
b0, eV (barrier)	ϵ_1		mr, effective mass ratio	T, K degree		1.89E+008	6 years
2.9		3.9	0.5	300		2.84E+017	9 years
C	b					3.78E+008	12 years
1.0630E-006	2.3854E+008					4.73E+008	15 years
						9.08E+009	18 years
						6.62E+008	21 years
						7.57E+008	24 years
						8.51E+008	27 years
						9.46E+008	30 years

Lfg um	0.6000	Channel length of floating gate device
Wfg um	1000.0000	Channel width of floating gate device.
Hfg um	0.0900	Thickness of floating gate polysilicon conductor
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation
Ttunox A	80	Tunnel oxide thickness
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
Cfc FF	1089.5358	Capacitance between the floating gate and the control gate
Cfsx FF	0.4313	Capacitance between the floating gate and the silicon substrate
Cfd FF	0.1078	Capacitance between the floating gate and the drain
Cfs FF	0.7547	Capacitance between the floating gate and the source
Cfg FF	1090.8295	Total floating gate capacitance
Cr,wl	0.9988	Control gate to floating gate coupling ratio
Cr,src	0.0007	Source junction to floating gate coupling ratio
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)
Vfg,ini	-5.00	Initial floating charged voltage
Vd	0.00	Actual erase voltage (equal to applied + charge stored on the floating)
S	3.76E+016	Derived parameter in the floating gate "erase" equation
X	1.27E+011	Derived parameter in the floating gate "erase" equation



Figures 1E-1F

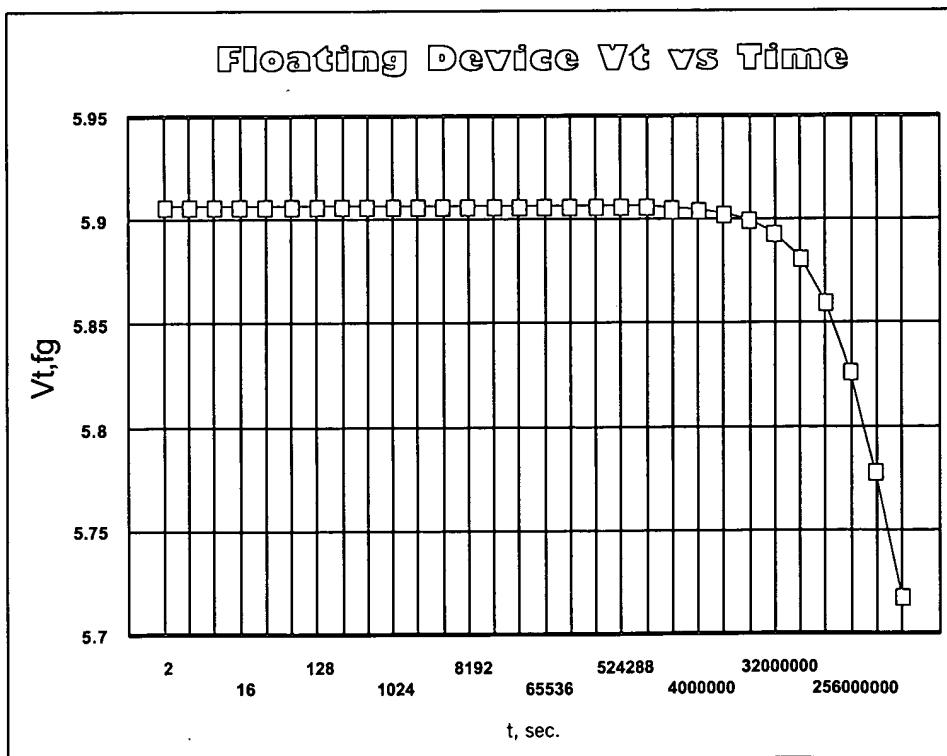
Calculation of memory cell retention characteristics

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	*****	3600	1 hour
b0, eV (barrier) ε1	mr, effective mass ratio		T, K degree	300	86400	1 day
2.9	3.9	0.5			604800	1 week
					2592000	1 month
C	b				*****	1 year
1.0630E-006	2.3854E+008				*****	4 years
					*****	16 years
					*****	32 years

Lfg um 0.6000 Channel length of floating gate device
 Wfg um 1000.0000 Channel width of floating gate device.
 Hfg um 0.0900 Thickness of floating gate polysilicon conductor
 Wrx um 0.5000 Width of floating gate overlapping shallow trench isolation
 Ttunox A 80 Tunnel oxide thickness
 Tono A 190 Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
 Tswox A 300 Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
 Xfd um 0.0500 Length of floating gate overlapping drain region of the floating gate MOSFET
 Xfs um 0.3500 Length of floating gate overlapping source region of the floating gate MOSFET
 Ainj um2 0.0438 Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge
 Cfc fF 1089.5358 Capacitance between the floating gate and the control gate
 Cfsx fF 0.4313 Capacitance between the floating gate and the silicon substrate
 Cfd fF 0.1078 Capacitance between the floating gate and the drain
 Cfs fF 0.7547 Capacitance between the floating gate and the source
 Cfg fF 1090.8295 Total floating gate capacitance
 Cr,wl 0.9988 Control gate to floating gate coupling ratio
 Cr,src 0.0007 Source junction to floating gate coupling ratio

 -Vt,fg V 0.90 Threshold voltage of floating gate MOSFET
 Verase 0.00 Erase voltage applied to the source(not used here, set to zero)
 -Vg,ini -5.00 Initial floating charged voltage
 -Vb 0.00 Actual erase voltage (equal to applied + charge stored on the floating)
 S 3.76E+016 Derived parameter in the floating gate "erase" equation
 X 1.27E+011 Derived parameter in the floating gate "erase" equation

t, sec. Vt,fg
 0.00001 5.907
 2 5.907
 4 5.907
 8 5.907
 16 5.907
 32 5.907
 64 5.907
 128 5.907
 256 5.907
 512 5.907
 1024 5.907
 2048 5.907
 4096 5.907
 8192 5.907
 16384 5.907
 32768 5.907
 65536 5.907
 131072 5.907
 262144 5.907
 524288 5.907
 1000000 5.907
 2000000 5.906
 4000000 5.905
 8000000 5.904
 16000000 5.900
 32000000 5.894
 64000000 5.881
 ***** 5.860
 ***** 5.827
 ***** 5.779
 ***** 5.718



Figures 1G-1H

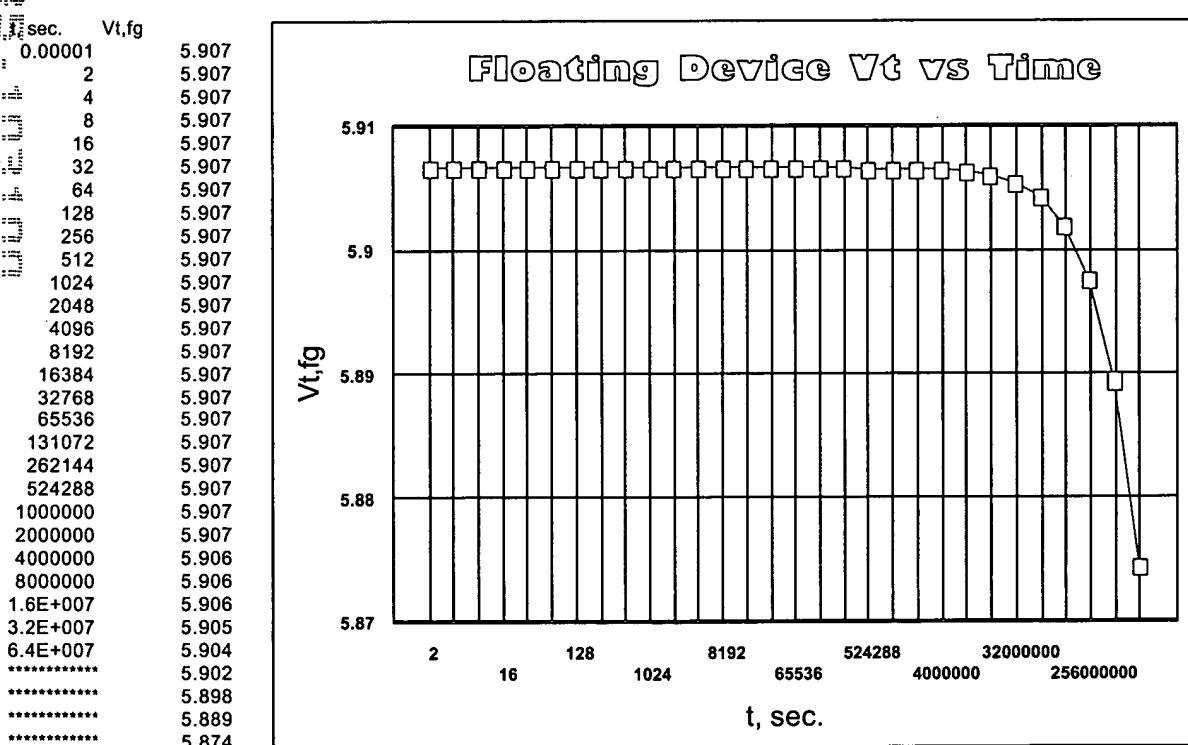
Calculation of Nv memory cell retention characteristics

q_0, C	m_0, kg	$kb, \text{J/K}$	$h, \text{J-s}$	$hb, \text{J-s}$	*****
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	*****	*****
$b_0, \text{eV (barrier)} \epsilon_1$		mr, effective mass ratio		T, K degree	
2.9		3.9		300	
C	b				
1.0630E-006	2.3854E+008				

Seconds	Time Period
60	1 minute
3600	1 hour
86400	1 day
604800	1 week
2592000	1 month
*****	1 year
*****	4 years
*****	16 years
*****	32 years

$L_{fg, um}$ 0.6000 Channel length of floating gate device
 $W_{fg, um}$ 1000.0000 Channel width of floating gate device.
 $H_{fg, um}$ 0.0900 Thickness of floating gate polysilicon conductor
 $W_{rx, um}$ 0.5000 Width of floating gate overlapping shallow trench isolation
 $T_{tunox, A}$ 85 Tunnel oxide thickness
 $T_{ono, A}$ 190 Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling
 $T_{swox, A}$ 300 Thickness of sidewall oxide between floating gate and control gate for sidewall coupling
 $X_{fd, um}$ 0.0500 Length of floating gate overlapping drain region of the floating gate MOSFET
 $X_{fs, um}$ 0.3500 Length of floating gate overlapping source region of the floating gate MOSFET
 A_{inj, um^2} 0.0438 Area of the electron tunneling region between the floating gate and the source for resetting the floating gate
 $C_{fc, fF}$ 1089.5358 Capacitance between the floating gate and the control gate
 $C_{fsx, fF}$ 0.4059 Capacitance between the floating gate and the silicon substrate
 $C_{fd, fF}$ 0.1015 Capacitance between the floating gate and the drain
 $C_{fs, fF}$ 0.7103 Capacitance between the floating gate and the source
 $C_{fg, fF}$ 1090.7534 Total floating gate capacitance
 $C_{r, wl}$ 0.9989 Control gate to floating gate coupling ratio
 $C_{r, src}$ 0.0007 Source junction to floating gate coupling ratio

 $V_{t, fg, V}$ 0.90 Threshold voltage of floating gate MOSFET
 V_{erase} 0.00 Erase voltage applied to the source(not used here, set to zero)
 $V_{fg, ini}$ -5.00 Initial floating charged voltage
 V_a 0.00 Actual erase voltage (equal to applied + charge stored on the floating)
 S 4.09E+017 Derived parameter in the floating gate "erase" equation
 X 1.20E+011 Derived parameter in the floating gate "erase" equation



Figures 1I-1J

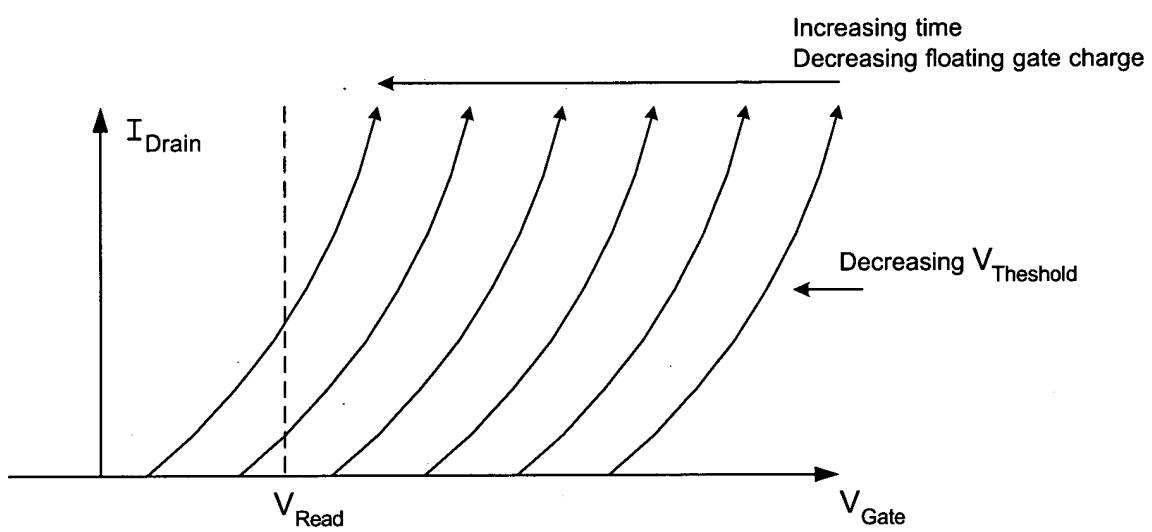
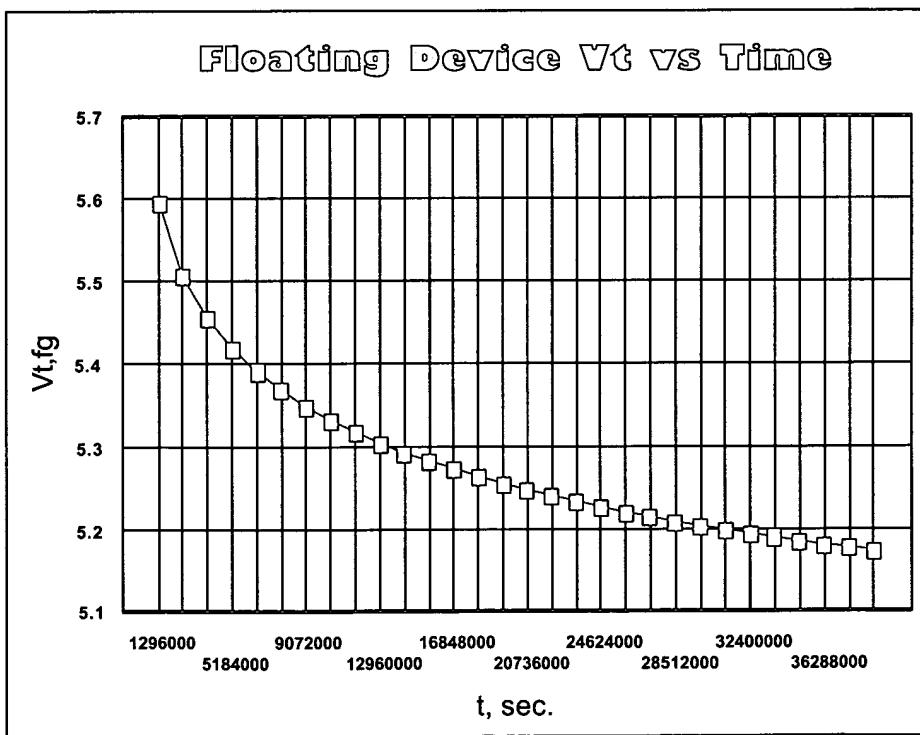


Figure 1K

Calculation of time cell retention characteristics

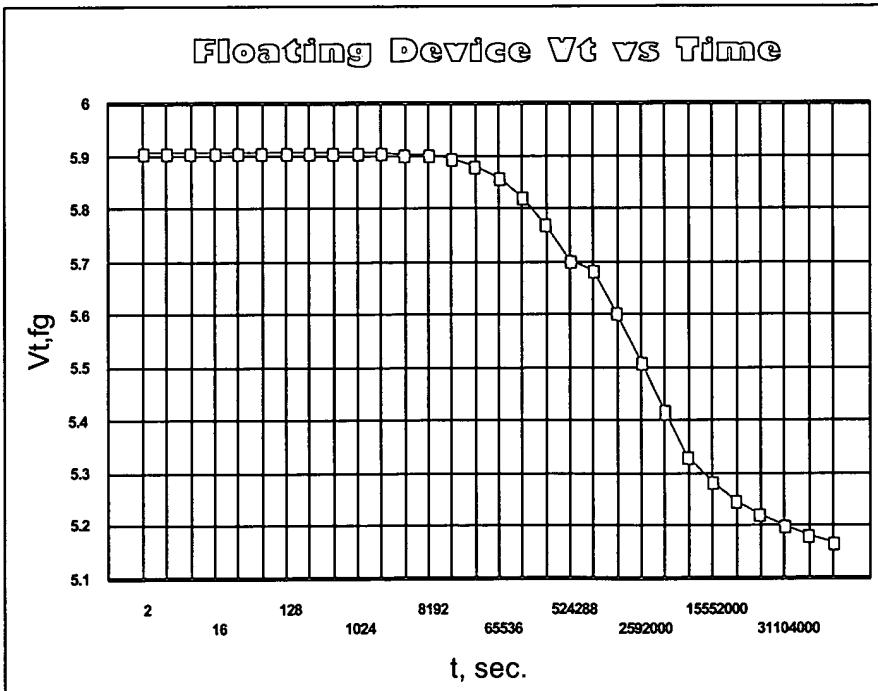
					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	2592000	1 month
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	*****	5184000	2 months
					7776000	3 months
b0, eV (barrier) ϵ_1		mr, effective mass ratio	T, K degree		*****	4 months
2.9	3.9	0.5	300		*****	5 months
C	b				*****	6 months
1.0630E-006	2.3854E+008				*****	7 months
					*****	8 months
					*****	9 months
					*****	10 months
					*****	11 months
					*****	12 months
					*****	13 months
Lfg um	0.6000	Channel length of floating gate device			*****	
Wfg um	1000.0000	Channel width of floating gate device.			*****	
Hfg um	0.0900	Thickness of floating gate polysilicon conductor			*****	
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation			*****	16 months
Ttunox A	65	Tunnel oxide thickness				
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling				
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling				
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET				
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET				
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge				
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate				
Cfsx fF	0.5308	Capacitance between the floating gate and the silicon substrate				
Cfd fF	0.1327	Capacitance between the floating gate and the drain				
Cfs fF	0.9288	Capacitance between the floating gate and the source				
Cfg fF	1091.1281	Total floating gate capacitance				
Crwl	0.9985	Control gate to floating gate coupling ratio				
Crsrc	0.0009	Source junction to floating gate coupling ratio				
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET				
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)				
Vfg,ini	-5.00	Initial floating charged voltage				
Va	0.00	Actual erase voltage (equal to applied + charge stored on the floating)				
S	2.93E+013	Derived parameter in the floating gate "erase" equation				
X	1.56E+011	Derived parameter in the floating gate "erase" equation				
t, sec.	Vt,fg					
0.00001	5.909					
1296000	5.596					
2592000	5.508					
3888000	5.456					
5184000	5.420					
6480000	5.392					
7776000	5.369					
9072000	5.349					
*****	5.333					
1.3E+007	5.318					
*****	5.305					
*****	5.293					
*****	5.283					
*****	5.273					
*****	5.264					
*****	5.256					
*****	5.248					
2.2E+007	5.240					
*****	5.234					
*****	5.227					
*****	5.221					
*****	5.215					
*****	5.210					
*****	5.204					
*****	5.199					
*****	5.195					
*****	5.190					
3.5E+007	5.185					
*****	5.181					
*****	5.177					
*****	5.173					



Figures 1L-1M

Calculation of time cell retention characteristics

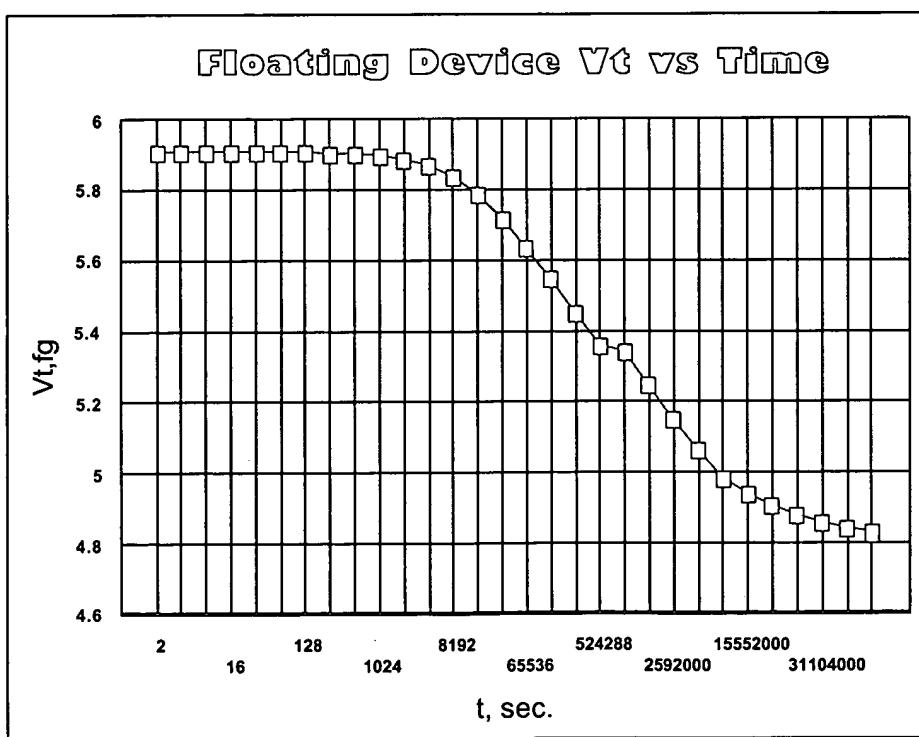
					Seconds	Time Periods
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	1.054588E-034	3600	1 hour
b0, eV (barrier)	el	mr, effective mass ratio	T, K degree		86400	1 day
2.9	3.9	0.5	300		604800	1 week
C	b				1209600	2 weeks
1.0630E-006	2.3854E+008				2592000	1 month
Lfg um	0.6000	Channel length of floating gate device			5184000	2 months
Wfg um	1000.0000	Channel width of floating gate device.			10368000	4 months
Hfg um	0.0900	Thickness of floating gate polysilicon conductor			15552000	6 months
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation			20736000	8 months
Ttunox A	65	Tunnel oxide thickness			25920000	10 months
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling			31104000	12 months
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling			36288000	14 months
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET			41472000	16 months
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET				
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge				
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate				
Cfsx fF	0.5308	Capacitance between the floating gate and the silicon substrate				
Cfd fF	0.1327	Capacitance between the floating gate and the drain				
Cfs fF	0.9288	Capacitance between the floating gate and the source				
Cfg fF	1091.1281	Total floating gate capacitance				
Cr,wl	0.9985	Control gate to floating gate coupling ratio				
Cr,src	0.0009	Source junction to floating gate coupling ratio				
Vt,fsg	0.90	Threshold voltage of floating gate MOSFET				
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)				
Vfg,ini	-5.00	Initial floating charged voltage				
Vs	0.00	Actual erase voltage (equal to applied + charge stored on the floating)				
S	2.93E+013	Derived parameter in the floating gate "erase" equation				
X	1.56E+011	Derived parameter in the floating gate "erase" equation				
Vt,fsg	5.909					
t, sec.	0.00001					
	2	5.909				
	4	5.909				
	8	5.909				
	16	5.909				
	32	5.909				
	64	5.909				
	128	5.909				
	256	5.908				
	512	5.908				
	1024	5.908				
	2048	5.907				
	4096	5.905				
	8192	5.902				
	16384	5.895				
	32768	5.883				
	65536	5.861				
	131072	5.824				
	262144	5.771				
	524288	5.702				
	1048000	5.666				
	2096000	5.604				
	4192000	5.508				
	8384000	5.420				
	16768000	5.333				
	33536000	5.283				
	67072000	5.248				
	134144000	5.221				
	268288000	5.199				
	536576000	5.181				
	1073152000	5.166				



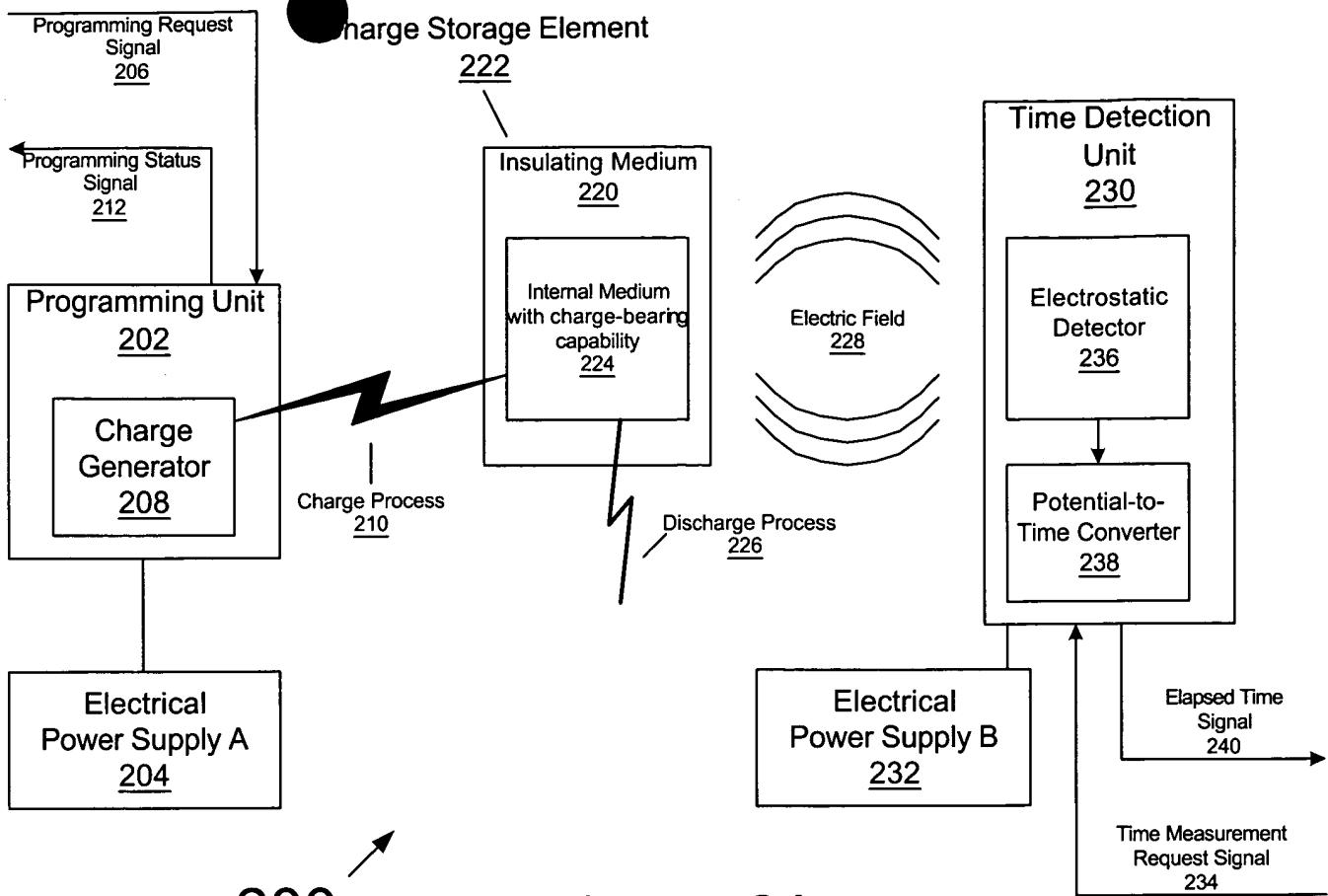
Figures 1N-10

Calculation of time cell retention characteristics

					Seconds	Time Period
q0, C	m0, kg	kb, J/K	h, J-s	hb, J-s	60	1 minute
1.6022E-019	9.1095E-031	1.38062E-023	6.62617E-034	*****	3600	1 hour
					86400	1 day
b0, eV (barrier) ϵ_1		mr, effective mass ratio	T, K degree		604800	1 week
2.9	3.9	0.5	300		1209600	2 weeks
C	b				2592000	1 month
1.0630E-006	2.3854E+008				5184000	2 months
					*****	4 months
					*****	6 months
					*****	8 months
					*****	10 months
					*****	12 months
					*****	14 months
					*****	16 months
Lfg um	0.6000	Channel length of floating gate device				
Wfg um	1000.0000	Channel width of floating gate device.				
Hfg um	0.0900	Thickness of floating gate polysilicon conductor				
Wrx um	0.5000	Width of floating gate overlapping shallow trench isolation				
Ttunox A	60	Tunnel oxide thickness				
Tono A	190	Thickness of Oxide-Nitride-Oxide dielectric between floating gate and control gate for capacitive coupling				
Tswox A	300	Thickness of sidewall oxide between floating gate and control gate for sidewall coupling				
Xfd um	0.0500	Length of floating gate overlapping drain region of the floating gate MOSFET				
Xfs um	0.3500	Length of floating gate overlapping source region of the floating gate MOSFET				
Ainj um2	0.0438	Area of the electron tunneling region between the floating gate and the source for resetting the floating gate charge				
Cfc fF	1089.5358	Capacitance between the floating gate and the control gate				
Cfsx fF	0.5750	Capacitance between the floating gate and the silicon substrate				
Cfd fF	0.1438	Capacitance between the floating gate and the drain				
Cfs fF	1.0063	Capacitance between the floating gate and the source				
Cfg fF	1091.2608	Total floating gate capacitance				
Crwl	0.9984	Control gate to floating gate coupling ratio				
Crsrc	0.0009	Source junction to floating gate coupling ratio				
Vt,fg V	0.90	Threshold voltage of floating gate MOSFET				
Verase	0.00	Erase voltage applied to the source(not used here, set to zero)				
Vfg,ini	-5.00	Initial floating charged voltage				
Vt	0.00	Actual erase voltage (equal to applied + charge stored on the floating)				
S	2.70E+012	Derived parameter in the floating gate "erase" equation				
X	1.69E+011	Derived parameter in the floating gate "erase" equation				
t, sec.	Vt,fg					
0.00001	5.909					
2	5.909					
4	5.909					
8	5.909					
16	5.909					
32	5.909					
64	5.909					
128	5.908					
256	5.907					
512	5.904					
1024	5.898					
2048	5.888					
4096	5.870					
8192	5.838					
16384	5.789					
32768	5.721					
65536	5.639					
131072	5.549					
262144	5.455					
524288	5.360					
604800	5.341					
1209600	5.250					
2592000	5.152					
5184000	5.067					
*****	4.985					
*****	4.938					
*****	4.906					
*****	4.881					
*****	4.861					
*****	4.844					
*****	4.830					



Figures 1P-1Q



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Figure 2A

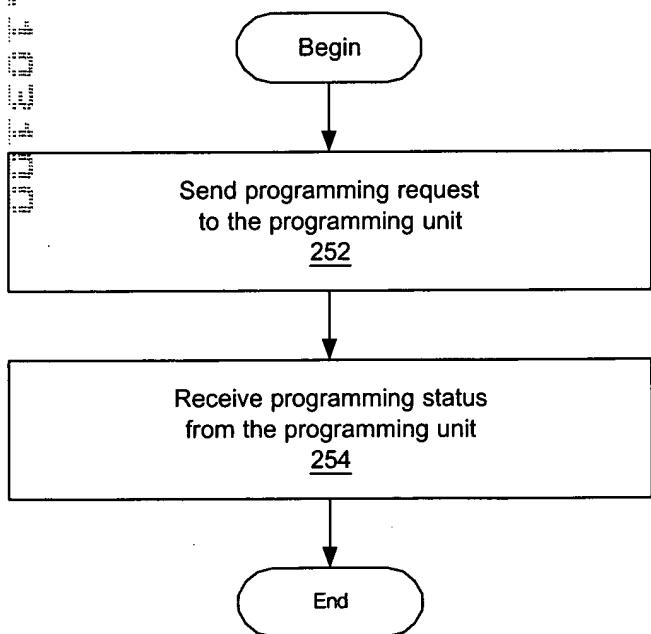


Figure 2B

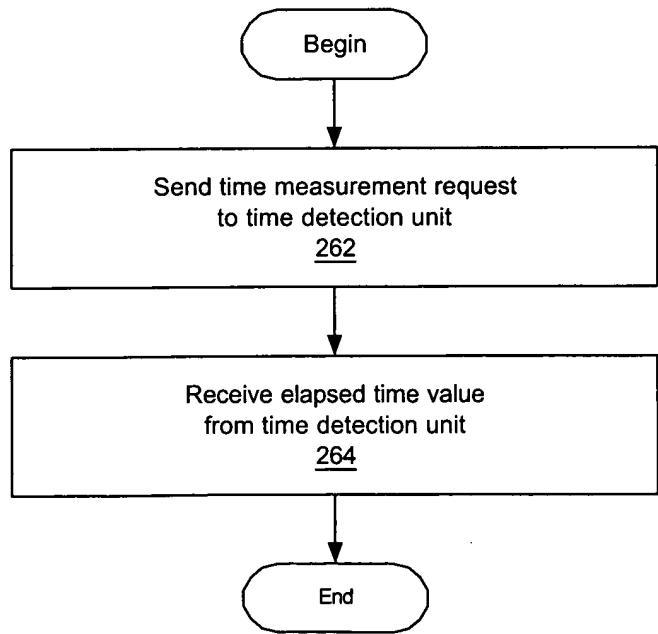


Figure 2C

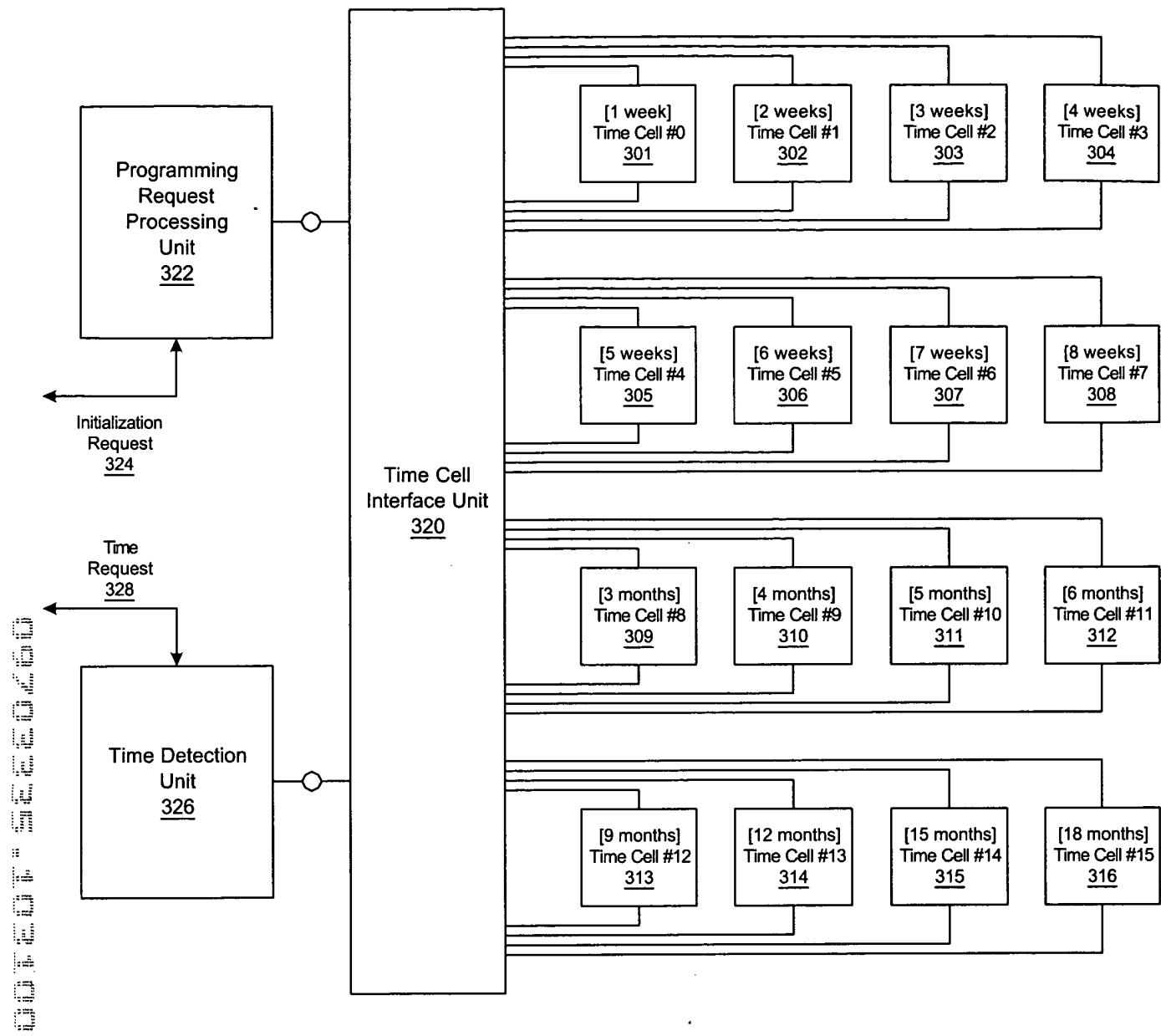


Figure 3A

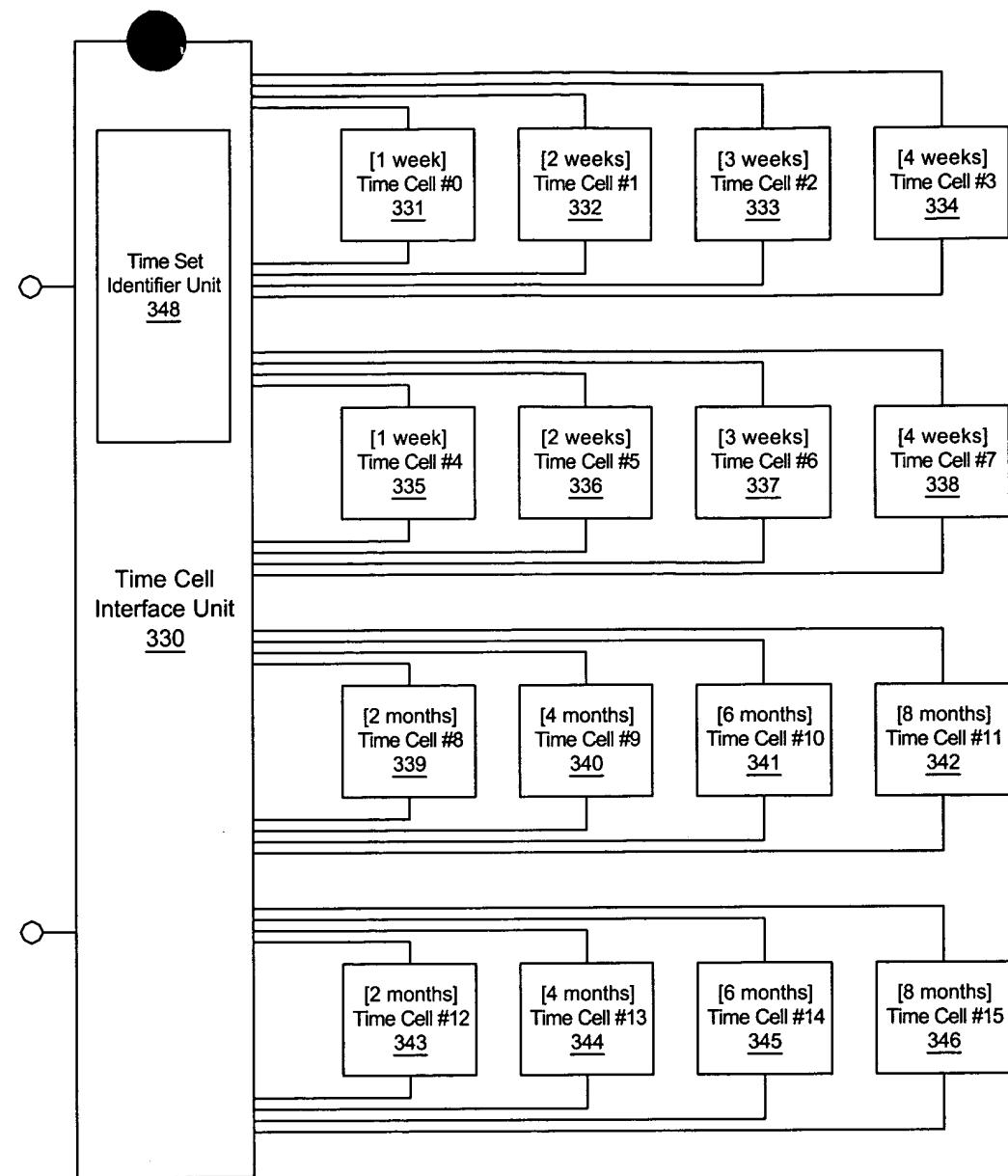


Figure 3B

00000000000000000000000000000000

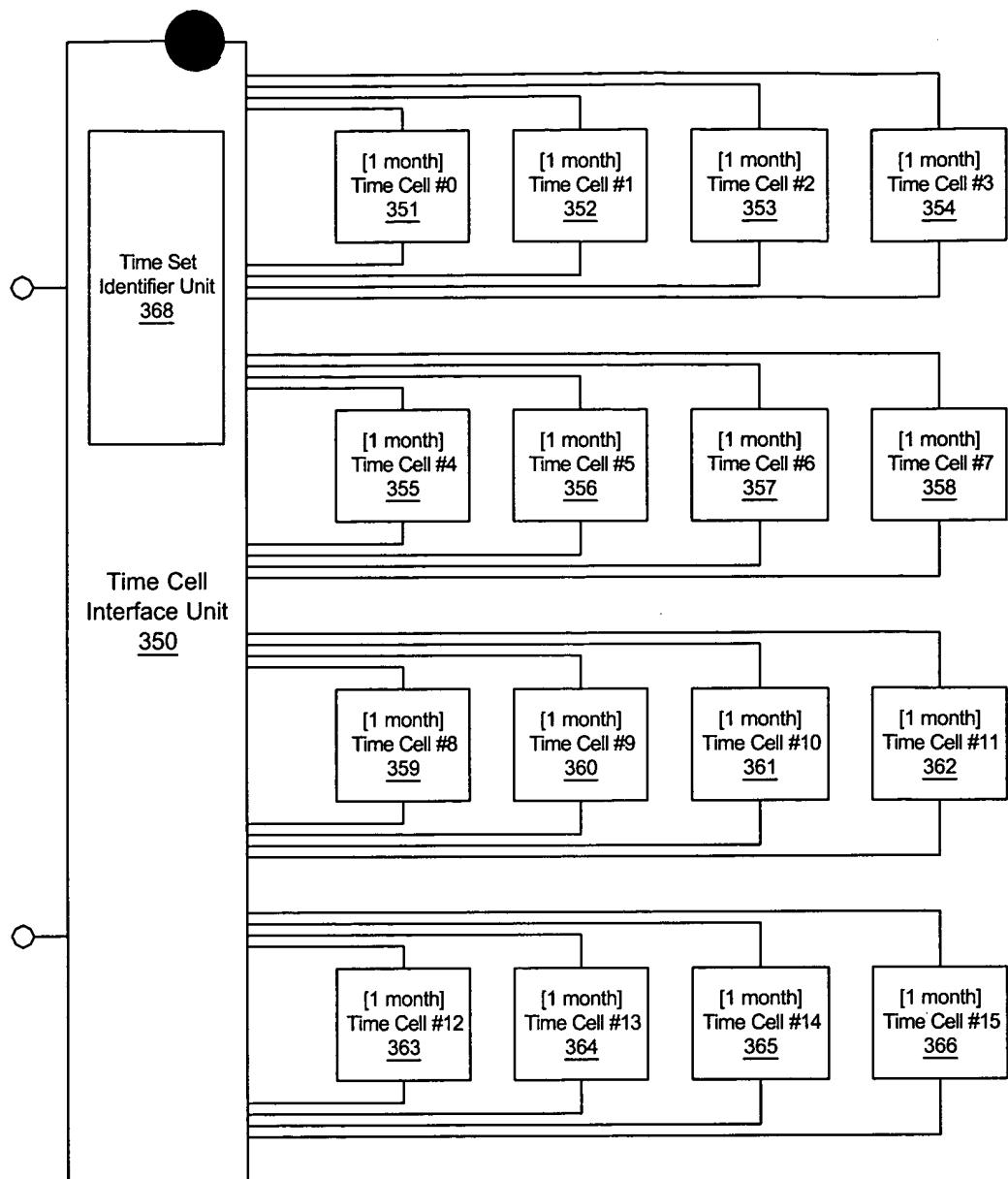


Figure 3C

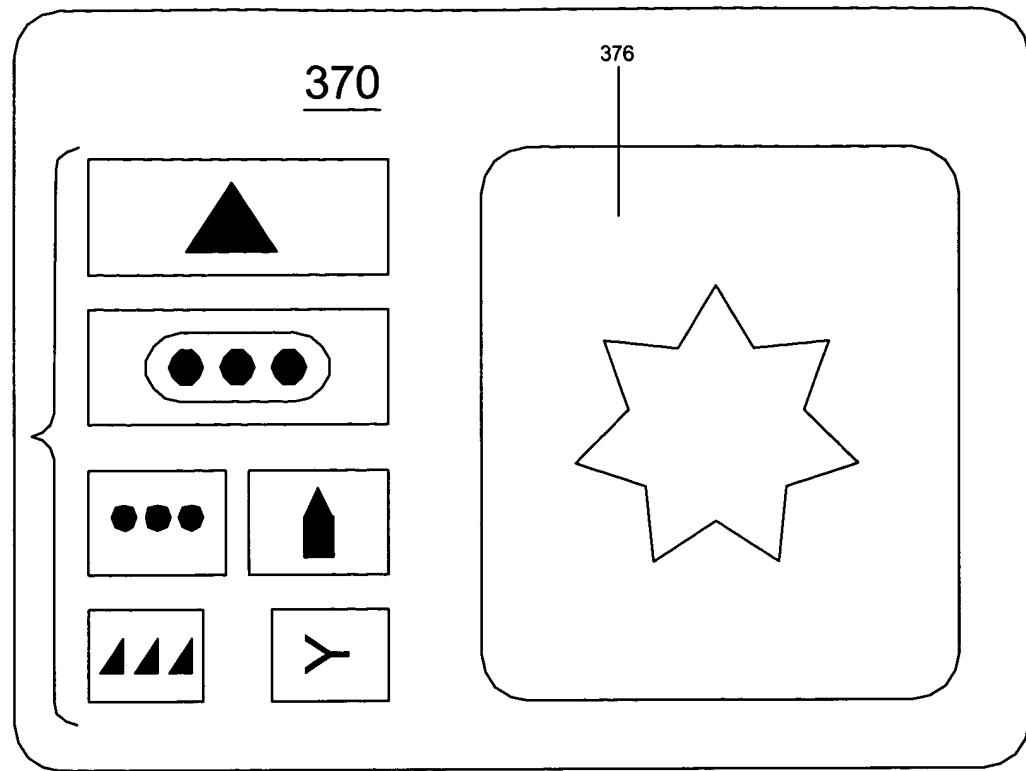


Figure 3D

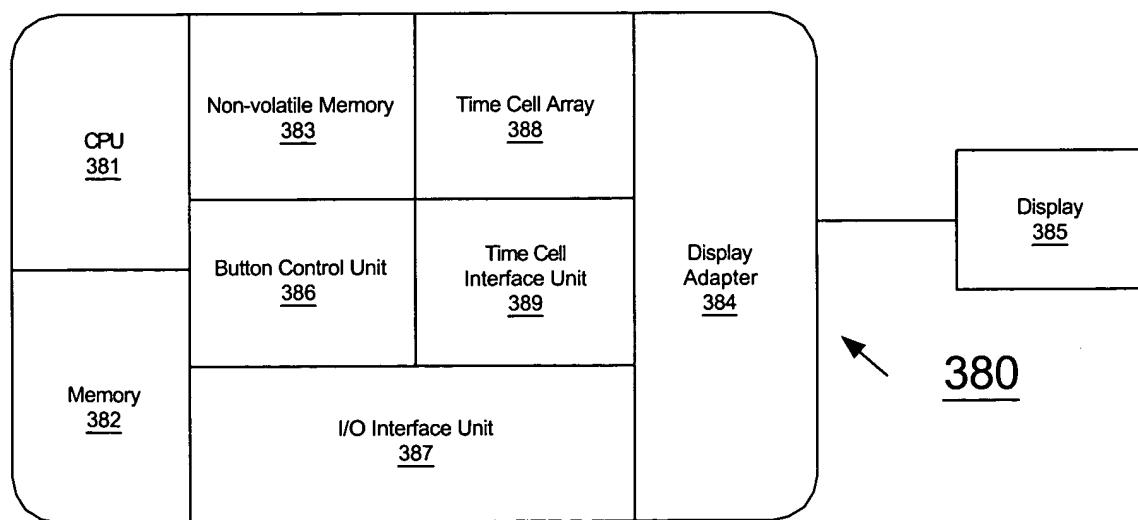


Figure 3E

390

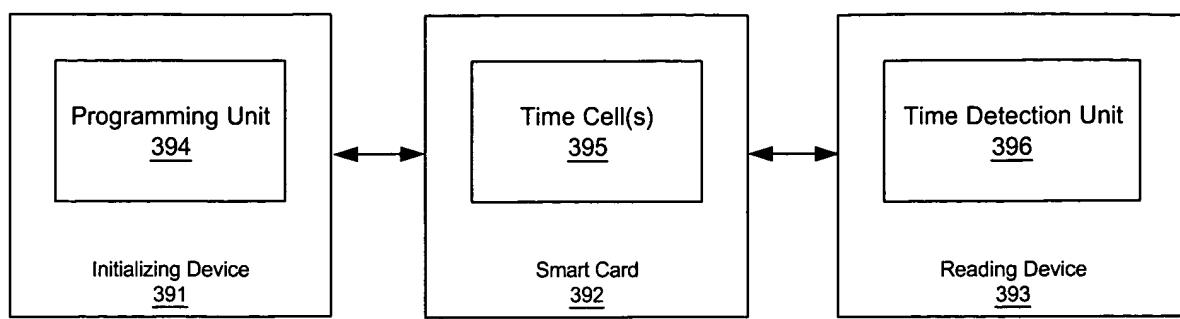


Figure 3F

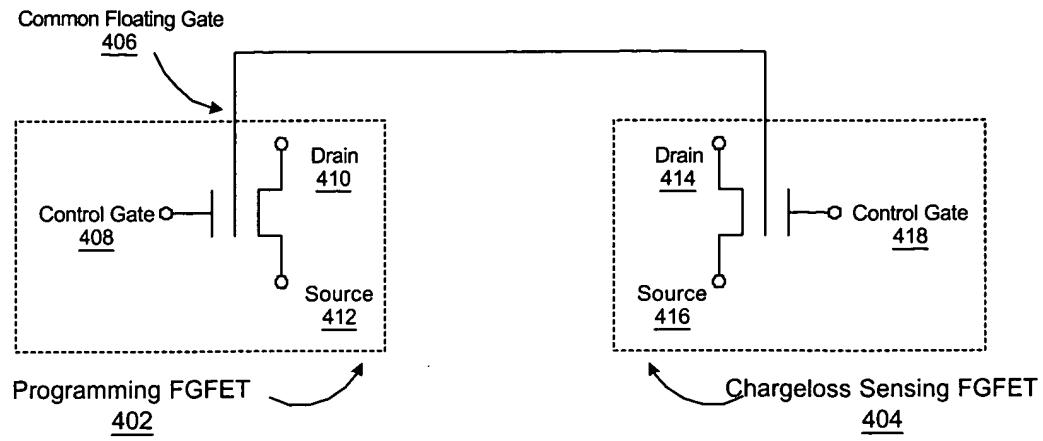


Figure 4A

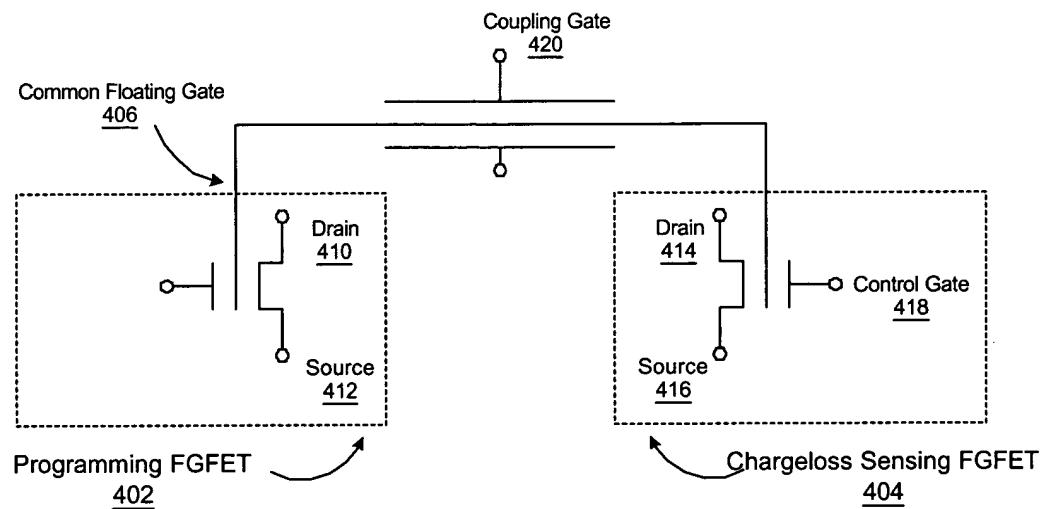


Figure 4B

Voltages during programming operation

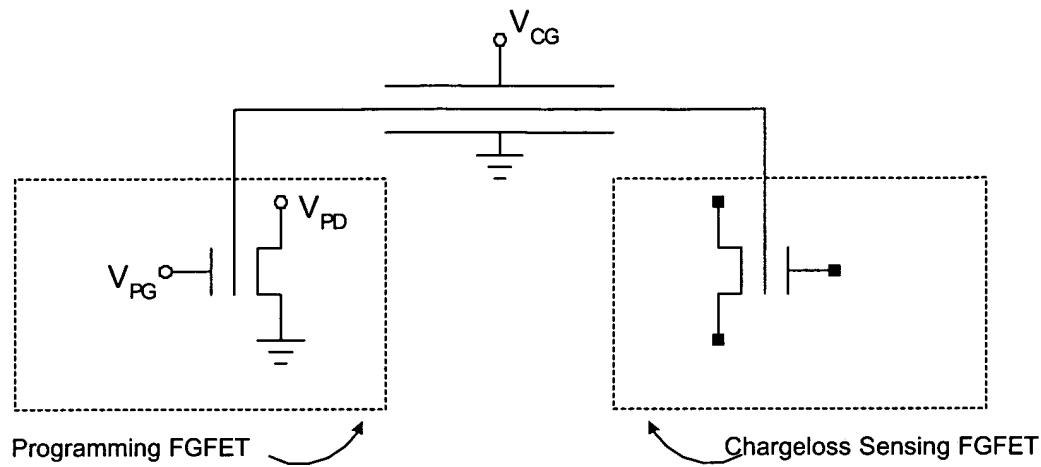


Figure 4C

Voltages during sensing operation

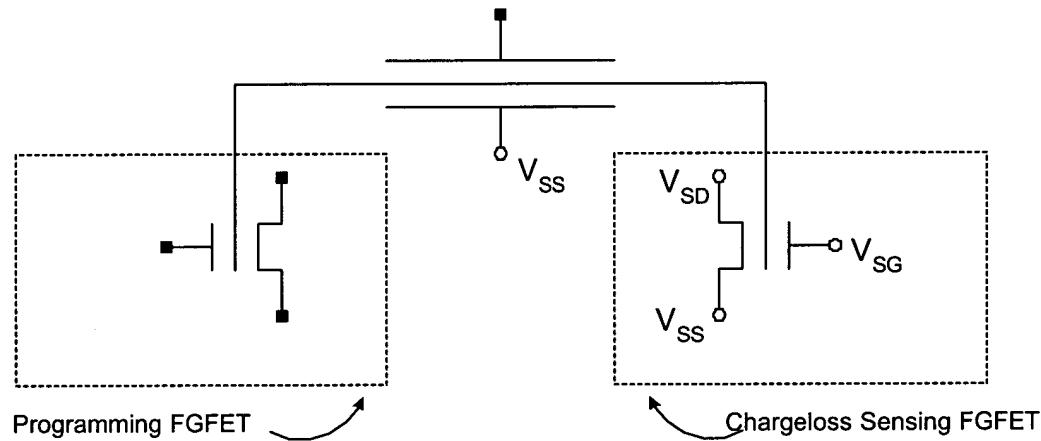


Figure 4D

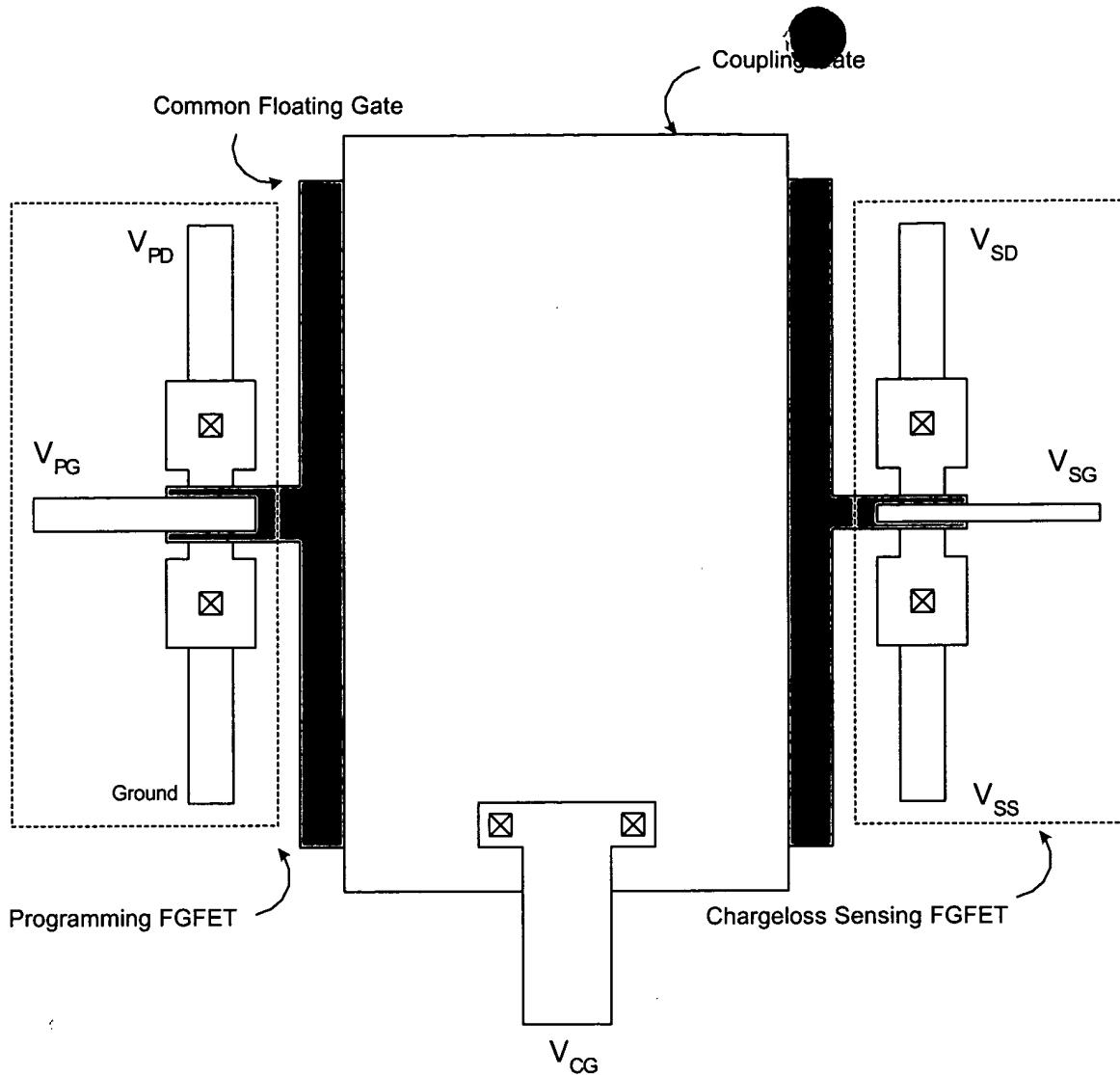


Figure 4E

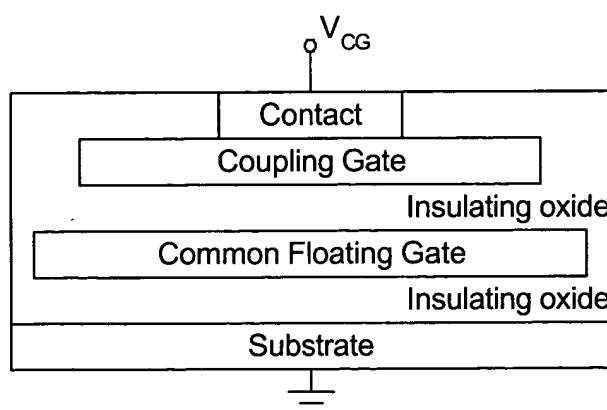


Figure 4F

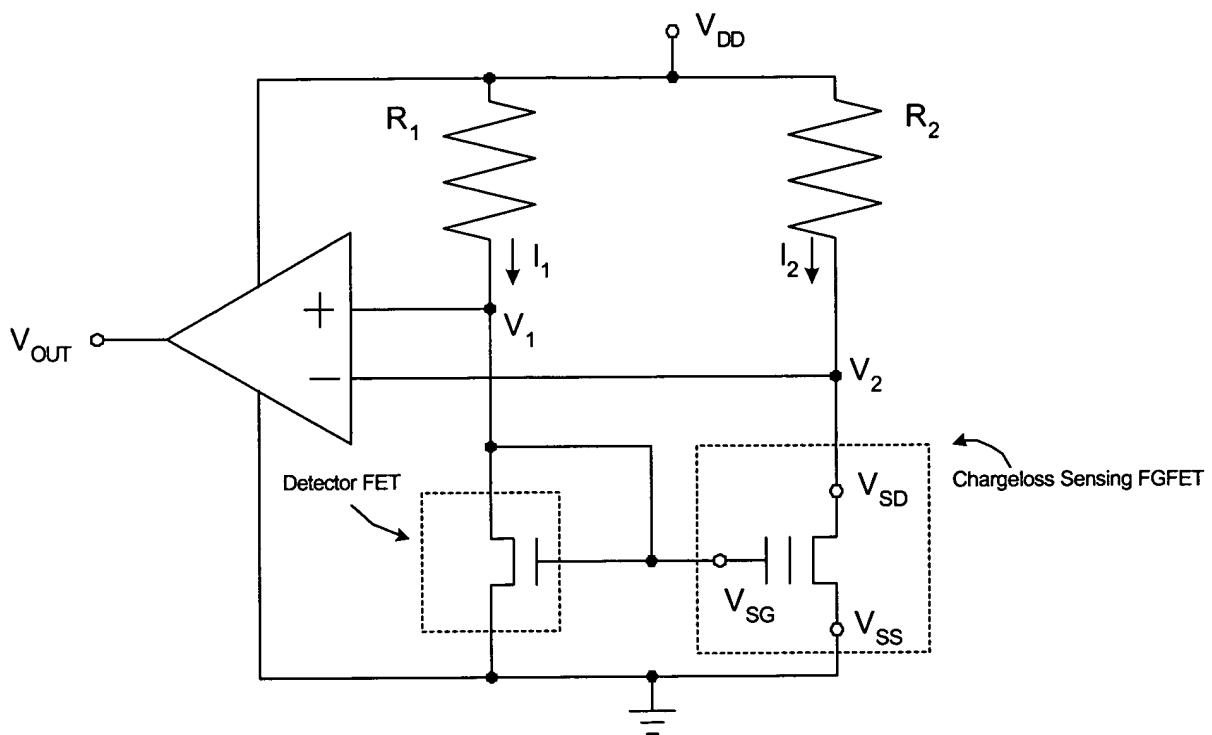


Figure 4G

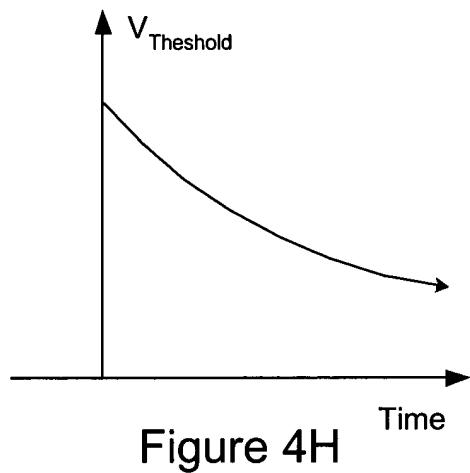


Figure 4H

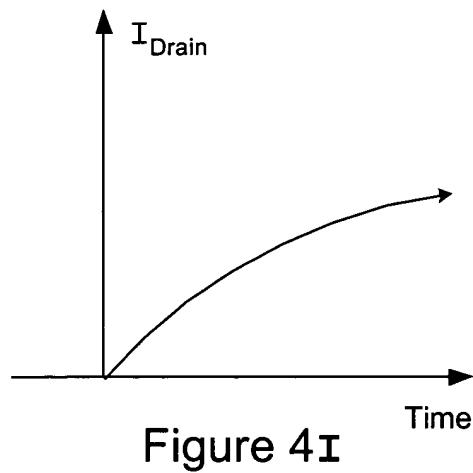


Figure 4I

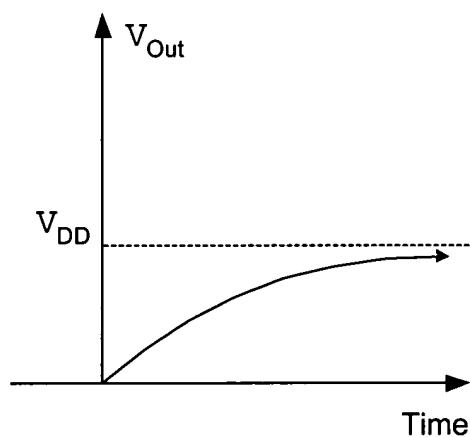


Figure 4J

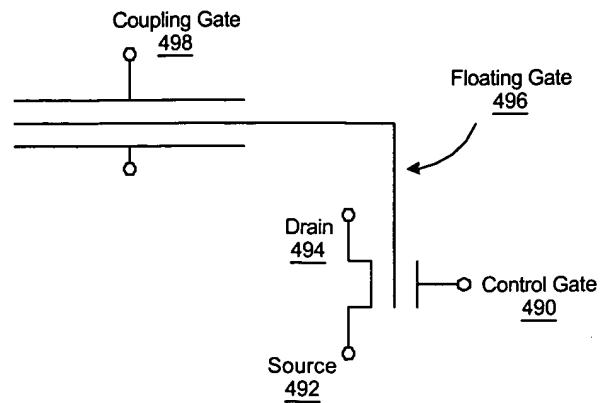


Figure 4M

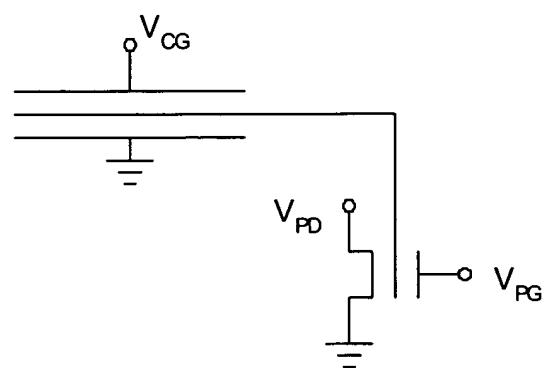


Figure 4N

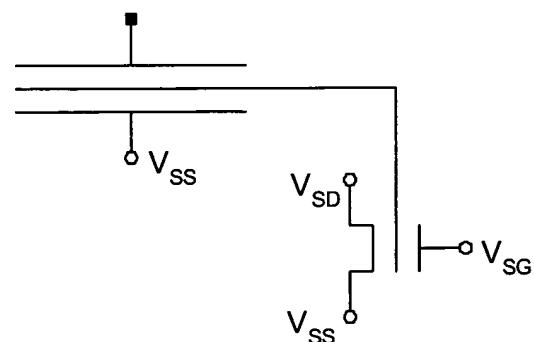


Figure 4O

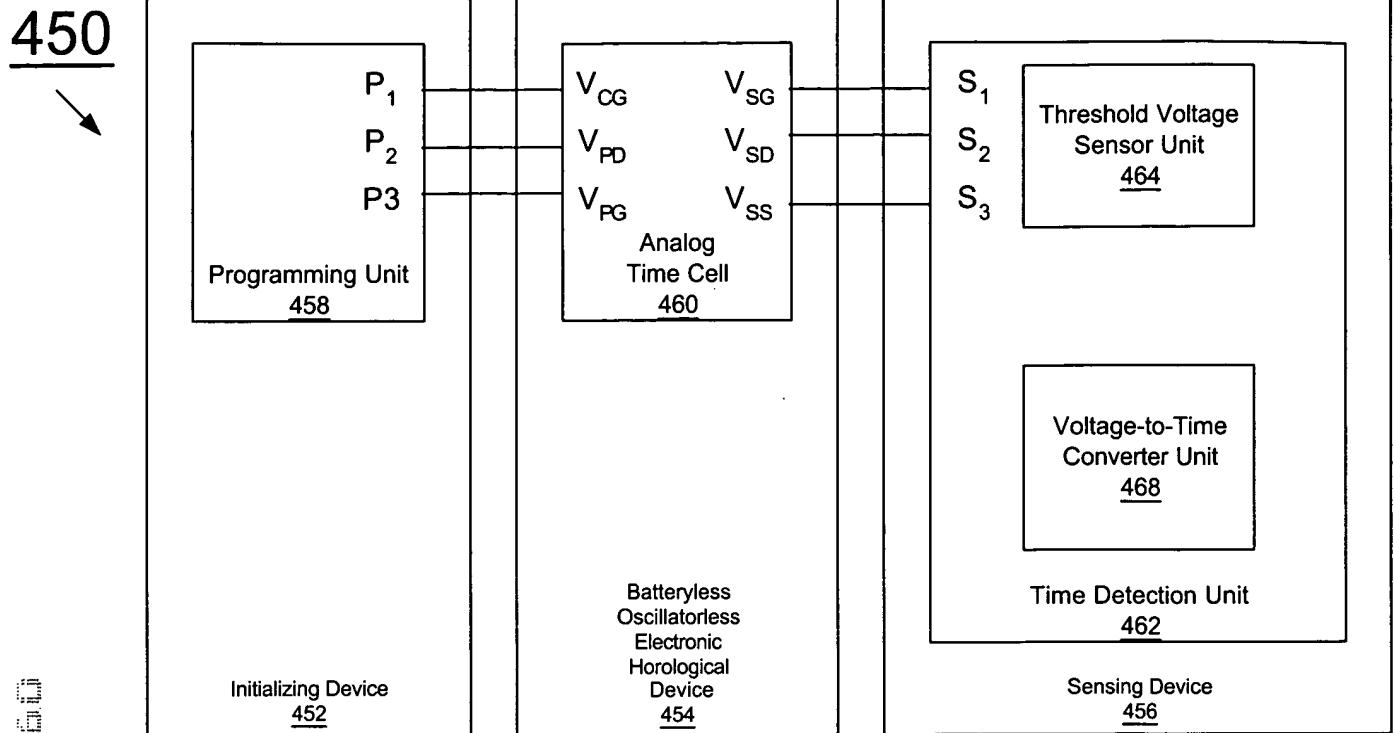


Figure 4K

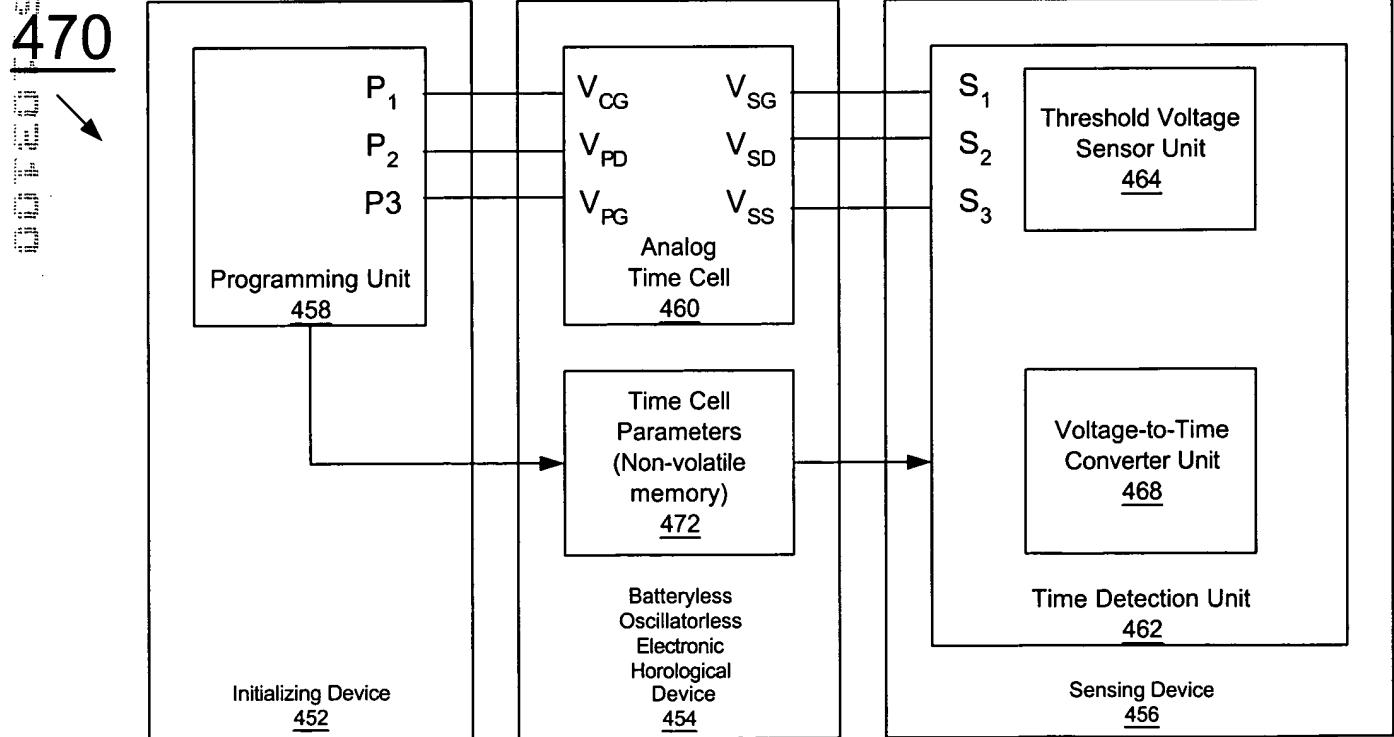


Figure 4L

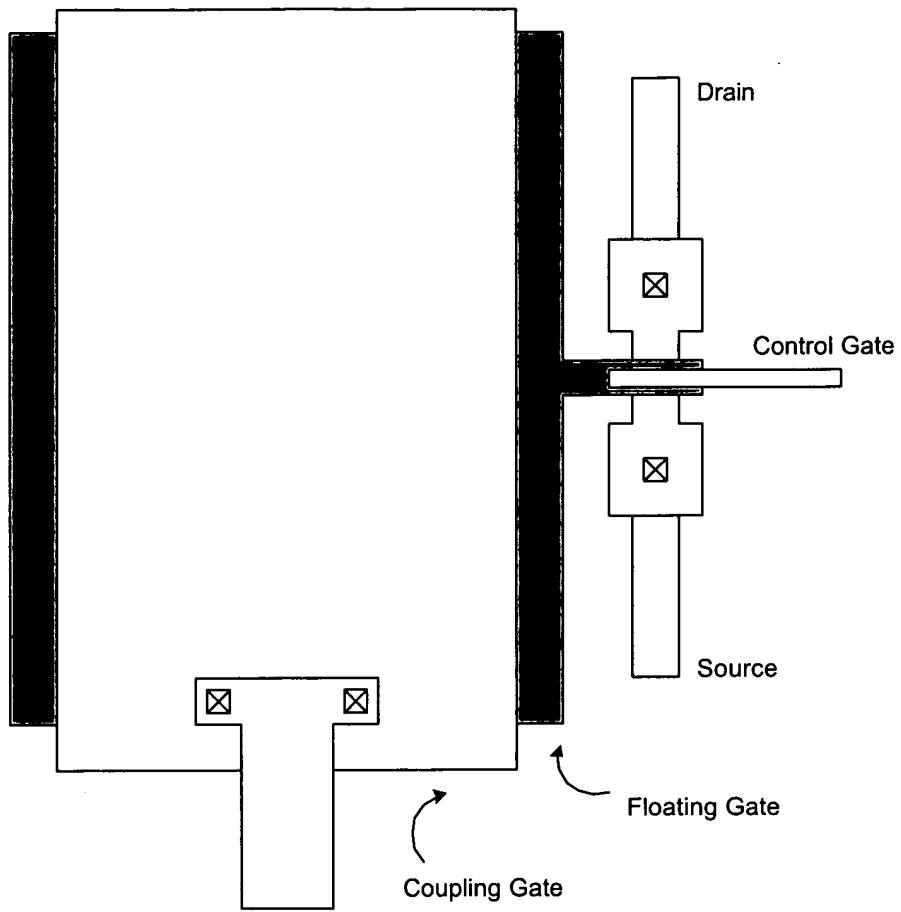


Figure 4P